Appl. No.: 10/79,101
Amdt. Dated July 26, 2005
Reply to Office Action Dated April 26, 2005

**Amendments to the Drawings**

The attached sheets of drawings include formal drawings for Figures 1-7 and reflecting changes to Figure 4 as suggested by the examiner. These sheets, which include Figures 1-7, replace the original sheets including Figures 1-7. In Figure 4, item 410 is illustrated.

## REMARKS

Claims 1-20 are pending in the application. Claims 1, 10-12, and 20 have been amended. Support for the amendments may be found throughout the specification, and particularly at pages 9-11. No new matter has been added. Applicants respectfully request favorable consideration and earnestly solicit allowance of the application in light of the above amendments and following remarks.

### Objections to the Drawings, Specification, and Claims

The objections to the drawings, Specification and claims have been obviated by appropriate amendments. Applicants have attached Formal drawings correcting the objections noted by the Examiner, and outlined in the Notice of Draftsperson's Patent Drawing review, attached to the Office Action.

### Rejections Pursuant 35 U.S.C. § 112

Amended claim 20 recites that reprogramming is effectuated by providing a voltage of opposite polarity. Accordingly, the rejection to claim 20 has been obviated by appropriate amendment.

### Rejections Pursuant 35 U.S.C. § 102

Claims 1-3, 10-14, and 16-20 have been rejected under 35 U.S.C. 102(e) as being anticipated by *Hsu, et al.* (US Pat. No. 6,617,737). Claims 1-10 and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by *Wang* (US Pat. No. 5,886,378). Applicants respectfully submit that neither *Hsu* nor *Wang* disclose the limitations of the pending claims.

Independent claim 1 relates to an electrically programmable transistor fuse having, *inter alia*, source and drain regions disposed in a substrate of semiconductor material having a first conductivity type. Independent claim 10 relates to a programmable fuse cell having, *inter alia*, source and drain regions also disposed in a substrate of semiconductor material having a first conductivity type. In the transistor fuse of claim 1 and the programmable fuse cell of claim 10,

the source and drain regions are spaced apart to define a channel region of the semiconductor material and insulating material having a uniform thickness is disposed over the source, drain and channel regions. Both the transistor fuse of claim 1 and the programmable fuse cell include two gates disposed in the single layer of polysilicon over the insulating material. The two gates are isolated from one another.

The cited reference to *Hsu*, on the other hand, does not disclose or suggest the limitations of either independent claim 1 or independent claim 10. Instead, *Hsu* relates to an electrically erasable programmable logic device (EEPLD) having a first and second PMOS transistors formed in an N-type well on a P-type semiconductor substrate. (Abstract) The first transistor has a floating gate and the second transistor has a select gate. (Abstract; col. 3, ll. 17-51). Figures 2a, 2b and 3 illustrate the layout of the EEPLD of *Hsu*. As illustrated in the figures, a P+ doped region 132 is disposed in a channel between the floating gate 122 and the select gate 124. (Col. 3, ll. 23-25). *Hsu* discloses that "by commonly using the P+ doped region 132, the PMOS transistors 101 and 102 are serially connected to each other." (Col. 3, ll. 42-44). Accordingly, *Hsu* describes that the two gates 122 and 124 are electrically connected by a doped region in the channel.

The cited reference to *Wang* also does not disclose or suggest the limitations of independent claims 1 and 10. *Wang* likewise related to an electrically erasable programmable read-only device (EEPROM) having a N regions 136 and 140 formed in a P-type substrate. (Figure 6; col. 2, l. 66 – col. 3, l. 3). The device of *Wang* includes a gate 156 and floating gate 160 each overlying the P-region between N-regions 136 and 140 of the substrate. (Col. 3, ll. 10-17). In the channel between N-regions 136 and 140 is N-region 138. *Wang* also discloses that the both the gate 156 and the floating gate 160 each overlay the N-region 138. (Figure 6). In addition, *Wang* discloses that N-region 138 is the source for transistor 162 and is "connected to the drain 138 of the first transistor 158." (Col. 3, ll. 17-23). The transistors 156 and 162 are also connected to each other though the connection of N-region 138 between gates 156 and 162. (Col. 3, ll. 42-44). Accordingly, *Wang* describes two gates that are electrically connected by a doped region in the channel.

Both *Hsu* and *Wang* disclose arrangements having gates that are electrically connected. Indeed, both disclose a region in the substrate in a channel between a source and a drain and

connected to the gates. The region connecting the gates is disposed between the gates. The gates of claims 1 and 10, on the other hand, are isolated where the channel region between the gates includes substrate material. Therefore, neither *Hsu* nor *Wang,* disclose a "first gate disposed overlapping a portion of said source region and said second gate isolated from said first gate," as recited in claims 1 and 10. Accordingly, limitations of claims 1 and 10 are entirely missing in the cited art. Applicants respectfully request reconsideration of the rejection of claims 1 and 10.

Dependent Claims 2-9 and 11-20

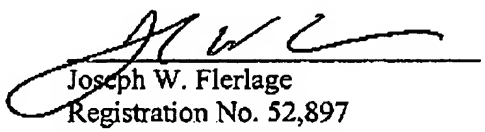
Applicants also respectfully submit that dependent claims 2-9 and 11-20 are not anticipated by the cited art. As discussed, limitations for independent claims 1 and 10 are not disclosed by the cited art. Therefore, the limitations of the claims dependent therefrom are also not disclosed or fairly suggested by the cited combination. Accordingly, Applicants respectfully submit that claims 2-9 and 11-20 are not anticipated.

## CONCLUSION

In view of the foregoing, Applicant respectfully requests favorable consideration and allowance for all pending claims. If the examiner believes that a telephone conference would expedite allowance of the application, the examiner is invited to call the undersigned.

Respectfully submitted,

July 26, 2005



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